

Figure 1

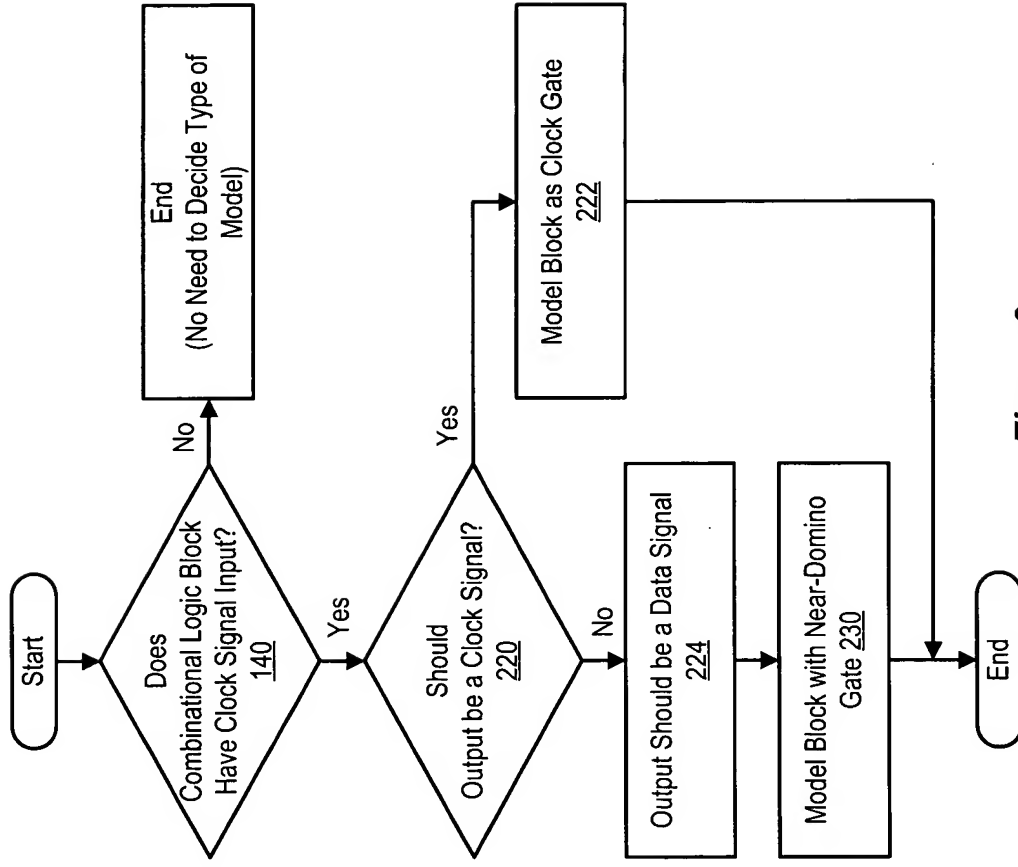


Figure 2

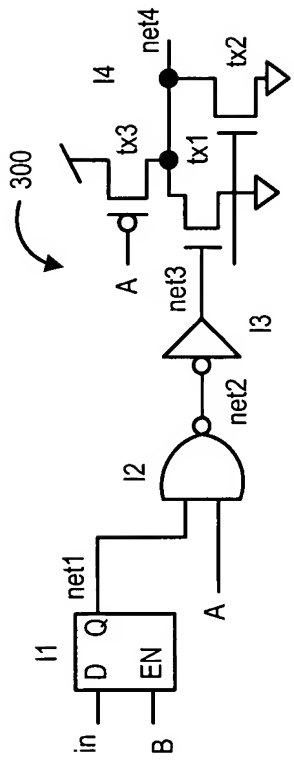


Figure 3

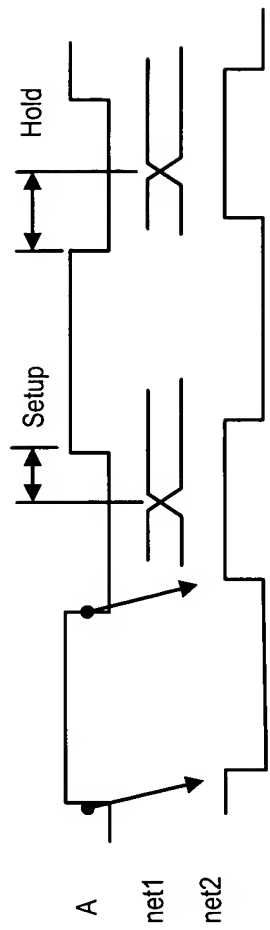


Figure 4

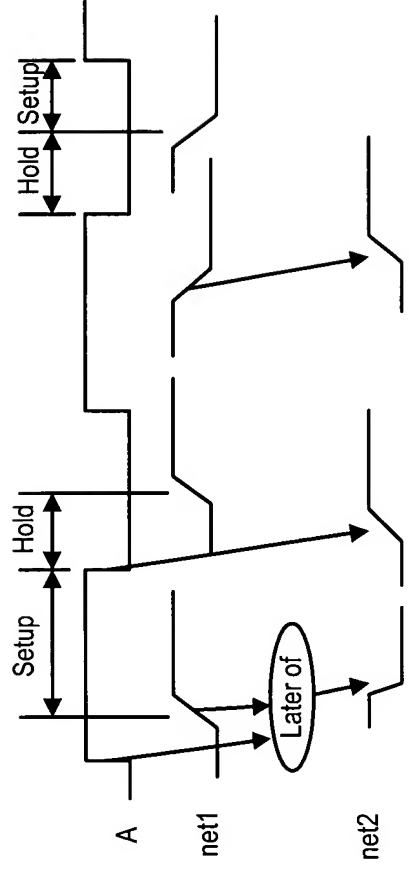


Figure 5

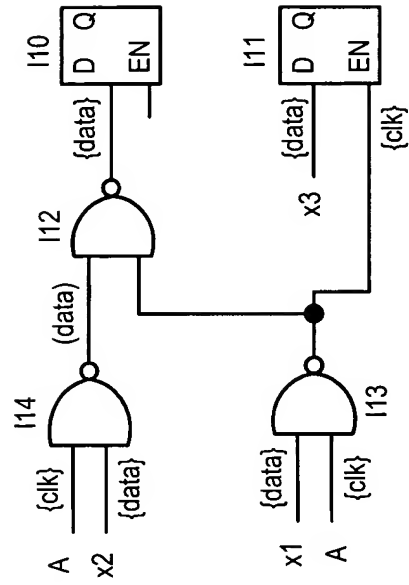


Figure 6

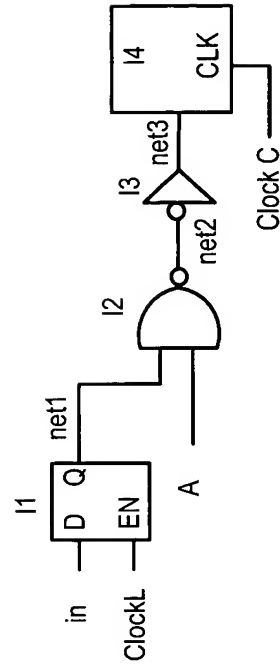


Figure 7

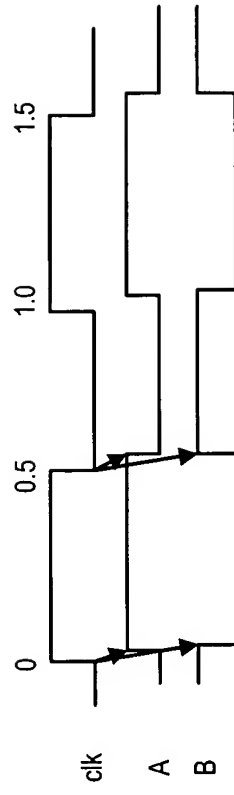


Figure 8

| Case | ClockL Phase | ClockC Phase | I4 | Clock Edge of Checks @ I2* | | | | Clock Edge of Checks @ I4* | | | |
|------|-----------------|-----------------|---------|----------------------------|-------|------|------|----------------------------|-------|------|------|
| | | | | su(r) | su(f) | h(r) | h(f) | su(r) | su(f) | h(r) | h(f) |
| 1 | B | A | Domino | 1.5 | 1 | 0.5 | 0.5 | 1.5 | 1 | 0.5 | 0.5 |
| 2 | B | B | Domino | 1.5 | 1 | 0.5 | 0.5 | 2 | 1.5 | 1 | 1 |
| 3 | A | A | Domino | 0.5 | 0 | 0.5 | 0.5 | 0.5 | 0 | 0.5 | 0.5 |
| 4 | A | B | Domino | 0.5 | 0 | 0.5 | 0.5 | 1 | 0.5 | 1 | 1 |
| 5 | B | A | Clkgate | 1.5 | 1 | 0.5 | 0.5 | 1 | 1 | 0.5 | 0.5 |
| 6 | B | B | Clkgate | 1.5 | 1 | 0.5 | 0.5 | 1.5 | 1.5 | 1 | 1 |
| 7 | A | A | Clkgate | 0.5 | 0 | 0.5 | 0.5 | 0 | 0 | 0.5 | 0.5 |
| 8 | A | B | Clkgate | 0.5 | 0 | 0.5 | 0.5 | 0.5 | 0.5 | 1 | 1 |
| 9 | B | A | Latch | 1.5 | 1 | 0.5 | 0.5 | 1.5 | 1.5 | 0.5 | 0.5 |
| 10 | B | B | Latch | 1.5 | 1 | 0.5 | 0.5 | 2 | 2 | 1 | 1 |
| 11 | A | A | Latch | 0.5 | 0 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| 12 | A | B | Latch | 0.5 | 0 | 0.5 | 0.5 | 1 | 1 | 1 | 1 |

Figure 9

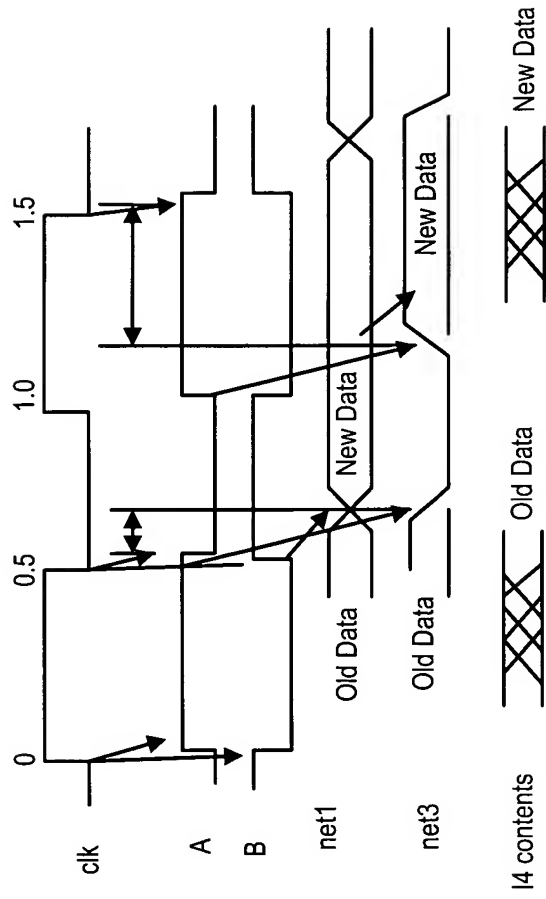


Figure 10